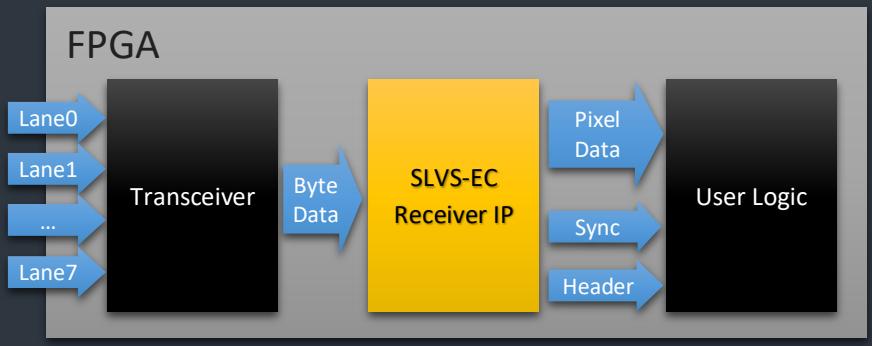
Introduction to CIS SLVS-EC Receiver IP

SLVS-EC Overview

SLVS-EC (Scalable Low Voltage Signaling with Embedded Clock) is a high speed, high performance interface for Sony CMOS image sensors. SLVS-EC differs from conventional LVDS interface in that the clock is embedded in the data, allowing circuit design without considering the pesky skew between serial buses. In a nutshell, SLVS-EC enables faster, lower power design made easy.

SLVS-EC Receiver IP Overview

CIS has concentrated on extracting pixel data from the byte data received via FPGA's high speed transceiver, enabling an IP with low FPGA resource usage , and also supports payload error detection and error correction (optional).



Specifications

Item	Compatibility
SLVS-EC Version	2.0 compliant
Lane	1,2,4,6,8
Raw Format	8,10,12,14,16
Line Length	4-∞ (default:65532)
CRC	Available
ECC	Available(optional)
Baud Rate	Grade1～3
Multi Stream	N.A.
Output Signals	Pixel Data, Sync. Signals, Packet Header etc.
Devices	AMD 7-Series, AMD Ultrascale, AMD Ultrascale+, Efinix Titanium, Efinix Topaz

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Resource Usage

One of the advantages of CIS's SLVS-EC Receiver IP is its low resource usage. Although this IP allows you to dynamically change the number of SLVS-EC lanes, which affects resource usage, you can further reduce resources by limiting the maximum number of lanes used or by using a fixed lane configuration. The resource usage in Artix7 (Vivado 2022.1) is as follows. Please contact us for resource usage when using other devices or tools.

Variable lane (ECC compatible in parentheses)

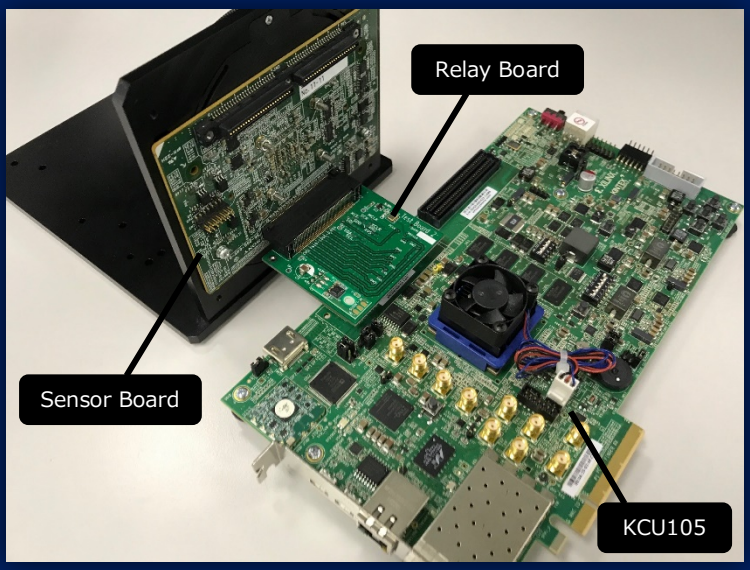
Resource	Max.2Lane	Max.4Lane	Max.8Lane
LUT	1116(2681)	1761(3829)	4165(6927)
FF	904(2351)	1253(3081)	1965(4523)
BRAM	0(2.5)	0(2.5)	0(3.5)

Fixed lane (ECC compatible in parentheses)

Resource	1lane	2lane	4lane	6lane	8lane
LUT	887(2181)	971(2430)	1323(3400)	2723(5576)	2290(5412)
FF	807(2250)	863(2308)	1155(2985)	1777(4329)	1816(4369)
BRAM	0(2.5)	0(2.5)	0(2.5)	0(3.5)	0(3.5)

Demonstration Environment

CIS provides relay boards for connecting SONY's IMX420 sensor board and AMD's evaluation boards, as well as reference designs for each evaluation board. For example, you can demonstrate Raw8, Raw10, and Raw12 using up to 2 lanes when using AC701, and up to 8 lanes when using KCU105 and ZCU106. Customers can freely customize and use the reference design. We also provide a demonstration environment for the Efinix Ti375N1156 evaluation board.



Support

CIS has many experienced engineers in the fields of RTL design related to various high-speed interfaces and image processing, board design including high-speed signals, and embedded software development, etc. Please feel free to contact us for IP customization, etc.

Contact

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